REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-14 remain in the application. Claims 10-14 have been withdrawn and rejoinder of claims 10-14 has been requested.

In item 1 on page 2 of the above-identified Office action, the Examiner has stated that the document "Optoelektronik I" submitted with the IDS on 9/13/2004 has not been considered because a concise explanation of the relevance is not provided.

Applicants enclose herewith a concise explanation of the relevance for the document "Optoelektronik I" and consideration of the document is requested.

It is noted that the Examiner has attached, with the Advisory action, a copy of the IDS of 9/13/2004 with his initial showing the consideration of the document "Optoelektronik I."

In item 2 on page 2 of the above-mentioned Office action, the Examiner has stated that the declaration filed 11/12/2004 under 37 CFR 1.131 is ineffective to overcome the Kinoshita (US PG-Pub 2003/0152125 A1) reference.

More specifically, the Examiner has stated that the evidence submitted is insufficient to establish diligence from a date prior to the date of reduction to practice of Kinoshita to either a constructive reduction to practice or an actual reduction to practice because no supporting evidence of any activity between the dates of 11/2/2001 and the filing date of the instant application has been submitted to establish due diligence.

It is not understood why Applicants have to establish due diligence between the dates of 11/2/2001 and the filing date of the instant application. Under 37 CFR 1.131, the critical period in which diligence must be shown begins just prior to the effective date of the reference and ends with the date of a reduction to practice, either actual or constructive. It is noted that the effective date of the Kinoshita reference is February 13, 2002 and the date of a constructive reduction to practice of the invention of the instant application is the priority date of July 31, 2002. Therefore, Applicants only need to establish due diligence between **February 12, 2002** and **July 31, 2002**. In order to perfect the priority, a certified English translation of the German application DE 102 34 976.2 is enclosed herewith.

The invention disclosure was received by the employer of the inventors on November 7, 2001 and it was decided on January 21, 2002 that a patent application should be filed. The patent attorney Mr. Schachtner, who is in charge of preparing the application document, sent a letter together with a draft application on **May 28, 2002** to one of the inventors Mr. Albrecht for reviewing the correctness and completeness thereof. The inventor Mr. Albrecht answered on **July 22, 2002** by fax and explained some points that need to be added to the draft. Both the attorney's letter on **May 28, 2002** and the inventor's answer on **July 22, 2002** are enclosed herewith as evidence.

Further, the Examiner is directed to the following passage in MPEP 715.07:

> *"The purpose of filing a [37 CFR 1.]131 affidavit is not to demonstrate prior invention, per se, but merely to antedate the effective date of a reference. See In re Moore, 58 CCPA 1340, 444 F.2d 572, 170 USPQ 260 (1971). Although the test for sufficiency of an affidavit under Rule 131(b) parallels that for determining priority of invention in an interference under 35 U.S.C. 102(g), it does not necessarily follow that Rule 131 practice is controlled by interference law. To the contrary, "[t]he parallel to interference practice found in Rule 131(b) should be recognized as one of convenience rather than necessity." Id. at 1353, 444 F.2d at 580, 170 USPQ at 267. Thus, "the 'conception' and 'reduction to practice' which must be established under the rule need not be the same*

> *as what is required in the 'interference' sense of those terms." Id.; accord, In re Borkowski, 505 F.2d 713, 718-19, 184 USPQ 29, 33 (CCPA 1974).*
>
> *. . . Also, in interference practice, conception, reasonable diligence, and reduction to practice require corroboration, whereas* ***averments made in a 37 CFR 1.131 affidavit or declaration do not require corroboration; an applicant may stand on his or her own affidavit or declaration if he or she so elects.*** *Ex parte Hook, 102 USPQ 130 (Bd. App. 1953)."*

In the Advisory action dated April 11, 2005, the Examiner has insisted that diligence is required for the time period between the dates of 11/2/2001 and the filing date of the instant US patent application. The Examiner has quoted the language from MPEP 715.07(a) as following:

> *Under* ***37 CFR 1.131****, the critical period in which diligence must be shown begins just prior to the effective date of the reference or activity and ends with the date of a reduction to practice, either actual or constructive (i.e., filing a United States patent application).*

However, this language does not exclude the filing of a foreign patent application to be considered as constructive reduction to practice. The term "i.e." is used here to provide an example, but not to exclude other possibilities. The fact that the phrase "i.e., filing a United States patent application" is placed in the parenthesis also shows that it is not exclusive.

This conclusion is also corroborated by other evidence found in the language of the patent rules and the MPEP. In pertinent part, 37 CFR 1.131 reads:

> (b) The showing of facts shall be such, in character and weight, as to establish reduction to practice prior to the effective date of the reference, or conception of the invention prior to the effective date of the reference coupled with due diligence from prior to said date to a subsequent reduction to practice or to the filing of the application.

It is noted that Rule 131 would have stated "the filing of a United States patent application" if it is so intended.

Below are some other quotes from the MPEP to show that the filing of a foreign patent application should be considered as constructive reduction to practice:

> *For additional examples of 35 U.S.C. 102(g) issues such as conception, reduction to practice and diligence outside the context of interference matters, see In re Costello, 717 F.2d 1346, 219 USPQ 389 (Fed. Cir. 1983) (discussing the concepts of conception and constructive reduction to practice in the context of a declaration under 37 CFR 1.131), and Kawai v. Metlesics, 480 F.2d 880, 178 USPQ 158 (CCPA 1973) (holding constructive reduction to practice for priority under 35 U.S.C. 119 requires meeting the requirements of 35 U.S.C. 101 and 35 U.S.C. 112).* MPEP 2138.

The critical period for diligence for a first conceiver but second reducer begins not at the time of conception of the first conceiver but just prior to the entry in the field of the party who was first to reduce to practice and continues until the first conceiver reduces to practice. Hull v. Davenport, 90 F.2d 103, 105, 33 USPQ 506, 508 (CCPA 1937) ("lack of diligence from the time of conception to the time immediately preceding the conception date of the second conceiver is not regarded as of importance except as it may have a bearing upon his subsequent acts"). What serves as the entry date into the field of a first reducer is dependent upon what is being relied on by the first reducer, e.g., conception plus reasonable diligence to reduction to practice (Fritsch v. Lin, 21 USPQ2d 1731, 1734 (Bd. Pat. App. & Inter. 1991), Emery v. Ronden, 188 USPQ 264, 268 (Bd. Pat. Inter. 1974)); an actual reduction to practice or a constructive reduction to practice by the filing of either a U.S. application (Rebstock v. Flouret, 191 USPQ 342, 345 (Bd. Pat. Inter. 1975)) or reliance upon priority under 35 U.S.C. 119 of a foreign application (Justus v. Appenzeller, 177 USPQ 332, 339 (Bd. Pat. Inter. 1971) (chain of priorities under 35 U.S.C. 119 and 120, priority under 35 U.S.C. 119 denied for failure to supply certified copy of the foreign application during pendency of the application filed within the twelfth month)). MPEP 2138.06.

Reduction to practice may be an actual reduction or a constructive reduction to practice which occurs when a patent application on the claimed invention is filed. The filing of a patent application serves as conception and constructive reduction to practice of the subject matter described in the application. Thus the inventor need not provide evidence of either conception or actual reduction to practice when relying on the content of the patent application. MPEP 2138.05. - Note the expression "a" patent application is used here.

In addition, it is noted in the case *In re Mulder and Wulms*, 219 USPQ 189 (Fed. Cir. 1983) mentioned by the Examiner during

a conversation with the counsel, the court has held that appellants are entitled to rely on their Netherlands filing date for a constructive reduction to practice.

> *If entitlement to a foreign filing date can completely overcome a reference we see no reason why it cannot partially overcome a reference by providing the constructive reduction to practice element of proof required by Rule 131. It is statutory priority right which cannot be interfered with by a construction placed on a PTO rule. In re Mulder and Wulms*, 219 USPQ 189 at 193.

In conclusion, the filing of the German application DE 102 34 976.2 on July 31, 2002 constitutes the constructive reduction to practice. Since the priority has been perfected and due diligence has been established for the period between the date February 12, 2002 just prior to the effective date of the Kinoshita reference and the date July 31, 2002 of the constructive reduction to practice of the invention of the instant application, it is believed that the Kinoshita reference is not available as prior art reference.

In item 4 on page 3 of the above-mentioned Office action, claims 1-9 have been rejected as being anticipated by Kinoshita under 35 U.S.C. § 102(e).

In view of the above discussion and evidence, it is clearly established that the invention of the instant application

antedates the Kinoshita reference. Therefore, the Kinoshita reference is not available as prior art and the Examiner's section 102 rejection on page 3 of the Office action is moot.

In view of the foregoing, reconsideration and allowance of claims 1-9 are solicited. Rejoinder of method claims 10-14 is requested upon allowance of product claims 1-9 under MPEP 821.04 ("if applicant elects claims directed to the product, and a product claim is subsequently found allowable, withdrawn process claims which depend from or otherwise include all the limitations of the allowable product claim will be rejoined").

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to

the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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Reg. No. 56,150

Yonghong Chen

For Applicants

YC

April 26, 2005

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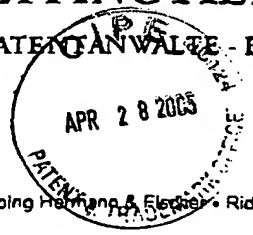
Concise explanation of the relevance of "Optoelektronik I"

This document was originally submitted to the Examiner in Taiwanese Patent Office to explain the DLDs (Dark Line Defects) mentioned in the specification of the instant application. This document describes on pages 300 and 301 the ageing of the luminescent diodes and the formation of dislocation lines along the principal crystal directions (compare page 301, lines 10-14). In contrast to the invention of the instant application, this document describes the application of defect-free substrates or the selection of the finished semiconductor layers (or the finished semiconductor components) to avoid this kind of defect.

EPPING HERMANN & FISCHER

PATENTANWÄLTE - EUROPEAN PATENT ATTORNEYS - EUROPEAN TRADEMARK ATTORNEYS



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Ihr Zeichen	Unser Zeichen	München,
605	E2001,0705 DE E (ML/GS)	28-Mai-2002

Erfindung „Verbesserung der Alterungsstabilität bei VCSEL"

Sehr geehrter Herr Albrecht,

anbei erhalten Sie den Entwurf für eine Patentanmeldung zur oben genannten Erfindung.

Wir möchten Sie bitten, diesen hinsichtlich technischer Vollständigkeit und Richtigkeit - evtl. unter Einbeziehung der Miterfinder - genau zu überprüfen, gegebenenfalls zu korrigieren oder zu ergänzen.

Sofern Sie mit der vorgeschlagenen Fassung einschließlich etwaiger Änderungsvorschläge einverstanden sind, unterzeichnen Sie bitte die beiliegende Erklärung und senden sie diese an uns zurück. Für den Eingang Ihrer Antwort haben wir uns den

11. Juni 2002

vorgemerkt. Für Rückfragen steht Ihnen der zuständige Bearbeiter gerne zur Verfügung.

Mit freundlichen Grüßen

Richard Schachtner
Patentanwalt

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Seiten Pages	1	Fax Fax	
Nummer Number		Datum Date	22.07.2002

Sehr geehrter Herr Lettenberger,

bezügliche der Erfindungsmeldung „Verbesserung der Alterungsstabilität bei VCSEL" E2001;0705DE E würden wir noch einige Punkte ergänzt/ verändert haben.

Zuerst muß ich mich jedoch wegen meiner sehr verspäteten Rückmeldung entschuldigen.

1. S.4 Beispiele für Materialverbindungen: InGaAlAs, InGaAlP, InGaAsP, InGaNAs
2. S.7 Eine Ausführungsform könnte wie folgt aussehen:
   Schchten 8, 11 (Braggspiegel) Paare aus $Al_{0.2}Ga_{0.8}As$/ $Al_{0.9}Ga_{0.1}As$ -Schichten
   Schicht 9 (aktive Schicht) 3 GaAs-QW für Emissionswellenlänge 850nm
   Schicht 10 (Stromeinschnürungsschicht) AlAs-Schciht, teilweise lateral oxidiert
   Schicht 12 (p-Kontakt) TiPtAu-Kontakt
   Schicht 13 (n-Kontakt) AuGe-Kontakt

Ich hoffe meine Erläuterungen können noch in den bestehenden Entwurf eingebaut werden. Für weitere Fragen stehe ich Ihnen gerne zur Verfügung.

Vielen Dank.

Mit freundlichen Grüßen

T. Albrecht

Docket No.: P2002,0637

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of the German Application No. 102 34 976.2 filed on July 31, 2002.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Hollywood, Florida

Carmen Panizzi

April 14, 2005

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P2002,0637

Description

Surface emitting semiconductor laser chip and method for producing it

The invention relates to a surface emitting semiconductor laser chip according to the preamble of patent claim 1 and to a method for producing it according to the preamble of patent claim 7.

Surface emitting semiconductor lasers are disclosed in DE 100 38 235.5, for example. What is characteristic of such lasers is an emission direction arranged perpendicular to the chip surface. These semiconductor lasers are often also referred to as VCSEL (Vertical Cavity Surface Emitting Laser). They differ in this in particular from so-called edge emitting lasers, in which the emission is effected through a side face of the laser chip.

In this case the designations "surface" and "side face" are associated with the fabrication of such chips in the wafer composite, the "surface" corresponding to the wafer surface. The side faces, by contrast, are only produced when the wafer is divided into individual semiconductor chips.

In a customary method for producing edge emitting laser chips, a wafer is usually broken in order to be divided into individual semiconductor chips, the breaking line running along a principal crystal direction of the wafer. This gives rise to side faces of the semiconductor bodies in the form of smooth cleavage faces which are simultaneously mirror facets of the respective laser resonators.

In the case of surface emitting lasers, the formation of such cleavage faces as side faces is not necessary on account of the different, perpendicular orientation of the resonator or emission direction. In order to produce such laser chips, therefore, the corresponding wafers can also be divided by sawing or etching instead of by breaking.

It has been ascertained in the case of light-emitting diode chips that a frequent ageing mechanism is based on dislocation lines arising in the semiconductor crystal. These dislocation lines can propagate during operation and form nonradiative recombination centers. Such crystal defects lower the efficiency of the device and may finally lead to failure. In the luminescent image of a semiconductor crystal, such crystal defects are seen as dark lines, and so they are also referred to as DLDs (dark line defects).

It is an object of the present invention to provide a surface emitting semiconductor laser chip having an improved ageing behavior or an increased lifetime. In particular, the intention is to reduce the production of nonradiative recombination centers or DLDs. Furthermore, it is an object of the invention to specify a corresponding production method.

This object is achieved by means of a surface emitting semiconductor laser chip according to patent claim 1 and a method according to patent claim 7. The dependent claims relate to advantageous developments of the invention.

The invention provides for the formation of a surface emitting semiconductor laser chip having a semiconductor body, which has, at least partly, a crystal structure with assigned principal crystal directions, a radiation exit face and side

faces laterally delimiting the semiconductor body, at least one side face being arranged obliquely, i.e. neither parallel nor perpendicular, with respect to the principal crystal directions. The radiation emission is effected during operation essentially perpendicular to the radiation exit face extending in the lateral direction.

Arranging the side faces obliquely with respect to the principal crystal directions has the advantage that fewer seeds for dislocation lines arise in the crystal structure and the number of dislocation lines thus decreases. This slows down the ageing of the semiconductor chip.

The semiconductor body preferably has a rectangular or square cross section parallel to the radiation exit face. This form can easily be fabricated from a wafer by sawing a wafer along sawing lines that cross one another orthogonally, it advantageously being possible for all the side faces to be arranged obliquely with respect to the principal crystal directions. In the invention, further preference is attached to at least one of the side faces being formed perpendicular to the radiation exit face.

The invention is suitable in particular for semiconductor materials having a cubic crystal structure, in which case, by way of example, without restricting the generality, the crystal directions [100] and [010] lie parallel to the radiation exit face and to the wafer surface, respectively. In this case, it is advantageous to arrange the side faces such that they form an angle of between 40° and 50°, preferably 45°, with the principal crystal directions [100] and [010].

In an advantageous refinement of the invention, the semiconductor body has a substrate in the form of a

semiconductor crystal, which defines the crystal directions, for example [100] and [010]. In this case, the laser structure is applied as a semiconductor layer sequence on said substrate. Such a layer sequence may be grown by means of an epitaxy method, for example.

The semiconductor body is preferably based on the GaAs/AlGaAs material system. In addition to said GaAs and AlGaAs, the semiconductor body may, of course, also contain other compounds such as, for example, AlGaInAs or InGaAs. Other III-V semiconductors or nitride compound semiconductors, for example the compounds GaP, InGaP, InAsP, GaAlP, InGaAlP, GaAsP, InGaAsP and InGaNAs are also suitable in the invention.

A production method according to the invention provides firstly for a wafer with a plurality of surface emitting semiconductor laser structures to be produced by means of a conventional fabrication method, the wafer having a crystal structure with principal crystal directions. The wafer is subsequently divided into a plurality of semiconductor laser chips along predetermined separating lines. These separating lines are arranged such that they run obliquely, that is to say neither parallel nor perpendicular, with respect to the principal crystal directions. The wafer is preferably sawn or divided by means of an etching method.

Arranging the separating lines obliquely with respect to the principal crystal directions advantageously reduces the formation of seeds for dislocation lines and, consequently, the production of ageing-accelerating dislocation lines or DLDs.

Further features, advantages and expediencies of the invention emerge from the following description of two exemplary embodiments in conjunction with Figs. 1 to 3, in which:

Fig. 1 shows a diagrammatic perspective view of a first exemplary embodiment of a surface emitting semiconductor laser chip according to the invention,

Fig. 2 shows a diagrammatic sectional view of the first exemplary embodiment, and

Fig. 3 shows a diagrammatic plan view of a second exemplary embodiment of a surface emitting semiconductor laser chip according to the invention.

Identical or identically acting elements are provided with the same reference symbols in the figures.

Fig. 1 diagrammatically shows a semiconductor laser chip of a VCSEL. The chip comprises a substrate 2, to which a stack of semiconductors layers 3 is applied. The semiconductor layers form the radiation-generating laser structure of the component in this case. This structure is explained in more detail below in connection with Fig. 2.

The semiconductor body 1 comprising the semiconductor layers 3 has a radiation exit face 4 and is laterally delimited by a plurality of side faces 5. During operation, the laser radiation 6 is emitted essentially in a direction perpendicular to the radiation exit face 4.

The substrate 2 and the semiconductor layers 3 applied thereto have, at least partly, a crystal structure. The crystal lattice in the lateral direction is illustrated by the broken

lines 16 and the associated principal crystal directions 7 are illustrated by arrows.

In the case of layers grown epitaxially, this structure is generally prescribed by the substrate. The principal crystal directions 7 of the semiconductor layers are thus also defined in a lateral direction. What is essential to the invention is that the side faces 5 are arranged such that they run obliquely with respect to the principal crystal directions 7, that is to say neither parallel nor perpendicular to said directions.

It has been ascertained in the context of the fabrication of LEDs that such an arrangement of the side faces 5 with respect to the principal crystal directions 7, in contrast to a parallel or perpendicular arrangement, advantageously reduces the formation of seeds for dislocation lines and an accompanying accelerated ageing of the component. Although the radiation-emitting region is significantly further away from the sawing track in the case of surface emitting semiconductor laser chips than in the case of LEDs, it has been found in the case of the invention that in this, too, the ageing of the component can advantageously be reduced by the invention's arrangement of the side faces with respect to the principal crystal directions.

Fig. 2 represents a sectional view along the line A-A through the exemplary embodiment shown in Fig. 1. A plurality of semiconductor layers 3 are arranged on the substrate 2, for example a GaAs substrate. This layer stack 3 comprises mirror layers 8, 11, which form the laser resonator and may be embodied as Bragg mirrors, for example. Such Bragg mirrors may be realized for example in each case as a layer sequence with alternate layers made of $Al_{0.2}Ga_{0.6}As$ and $Al_{0.9}Ga_{0.1}As$.

An active layer 9 is arranged between said mirror layers 8, 11. This active layer 9 is preferably designed as a quantum well structure, for example in the form of an SQW structure (Single Quantum Well) or an MQW structure (Multiple Quantum Well). An example of a suitable MQW structure is a structure having three GaAs quantum wells with an emission wavelength of about 850 nm.

The layer 10 is formed as a so-called current constriction layer which, during operation, guides the pumping current, represented by way of example using the current paths 15, toward the center of the active layer 9 and thus increases the pumping density of the laser. The current constriction layer may be formed as an AlAs layer; it is partly laterally oxidized.

In this case, an active radiation-emitting zone 14 arises in the center of the active layer 9, in which case, when the pumping threshold or the threshold current is exceeded, the laser starts to oscillate and emits laser radiation 6 in a direction perpendicular to the radiation exit face 4. For supplying the pumping current, contact metallizations 12, 13 are provided on the radiation exit face 4 and the opposite surface of the substrate 2. The contact metallization 12 is embodied as a ring contact, for example. The contact metallization 12 is preferably embodied as a p-contact, for example as a TiPtAu contact, and the contact metallization 13 as an n-contact, for example as an AuGe contact.

For the sake of clarity, said contact metallizations are not represented in Fig. 1.

Fig. 3 shows a diagrammatic plan view of a second exemplary embodiment of the invention. The semiconductor body 1 essentially corresponds to the exemplary embodiment represented in Fig. 1. A GaAs-based material is used as the semiconductor material. Without restricting the generality, the principal crystal directions [100] and [010] are arranged parallel to the radiation exit face 4. The semiconductor body 1 has a square cross section parallel to the radiation exit face 4, as shown by the plan view, and is laterally delimited by side faces 5. The side faces 5 in each case form an angle of 45° with the principal crystal directions [100] and [010].

It has been found that the ageing behavior of a corresponding component, such as a VCSEL, for example, can be significantly improved by means of an arrangement of this type.

Patent Claims

1. A surface emitting semiconductor laser chip having a semiconductor body (1) , which has, at least partly, a crystal structure with principal crystal directions (7), a radiation exit face (4) and side faces (5) laterally delimiting the semiconductor body (1),
characterized in that
at least one side face (5) is arranged obliquely with respect to the principal crystal directions (7).

2. The semiconductor laser chip as claimed in patent claim 1, characterized in that
the semiconductor body (1) has a square or rectangular cross section parallel to the radiation exit face (4).

3. The semiconductor laser chip as claimed in patent claim 1 or 2,
characterized in that
at least one of the principal crystal directions (7), in particular the [100] direction, runs parallel to the radiation exit face (4), and at least one of the side faces (5) forms an angle of between 40° and 50°, preferably an angle of 45°, with said principal crystal direction.

4. The semiconductor laser chip as claimed in one of claims 1 to 3,
characterized in that
the semiconductor laser chip comprises a substrate (2), which has, at least partly, a crystal structure.

5. The semiconductor laser chip as claimed in one of claims 1 to 4,
characterized in that

the semiconductor body contains a III-V compound semiconductor, in particular GaAs or AlGaAs, and/or a nitride compound semiconductor.

6. The semiconductor laser chip as claimed in one of claims 1 to 5,
characterized in that
the semiconductor laser chip is a VCSEL.

7. A method for producing a surface emitting semiconductor laser chip, in which a semiconductor wafer with a plurality of surface emitting semiconductor structures is produced, the semiconductor wafer having principal crystal directions and the semiconductor wafer being divided into a plurality of semiconductor laser chips along separating lines,
characterized in that
the separating lines are arranged obliquely with respect to the principal crystal directions.

8. The method as claimed in claim 7,
characterized in that
the semiconductor wafer is sawn or etched in the course of the dividing process along the separating lines.

9. The method as claimed in claim 7 or 8,
characterized in that
the separating lines form an angle of between 40° and 50°, preferably an angle of 45°, with the principal crystal directions.

10. The method as claimed in one of claims 7 to 9,
characterized in that
the semiconductor laser chip is a VCSEL.

Abstract

Surface emitting semiconductor laser chip and method for producing it

The invention describes a surface emitting semiconductor laser chip having a semiconductor body (1) , which has, at least partly, a crystal structure with principal crystal directions (7), a radiation exit face (4) and side faces (5) laterally delimiting the semiconductor body (1), at least one of the side faces (5) being arranged obliquely with respect to the principal crystal directions (7). The invention furthermore describes a method for producing such a semiconductor laser chip.

Fig. 1

nt